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(54) P-type group II-VI compound semiconductor crystals, growth method for such crystals, and semiconductor device made of such crystals

(57) A method of growing p-type group II-VI compound semiconductor crystals, includes a step of forming ZnO layers and ZnTe layers alternately on a ZnO substrate, the ZnO layer being not doped with impurities and having a predetermined impurity concentration, and the ZnTe layer being doped with p-type impurities N to a predetermined impurity concentration or higher.

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Description

[0001] This application is based on Japanese Patent Application HEI 11-142059, filed on May 21, 1999, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

a) Field of the Invention

[0002] The present invention relates to p-type group II-VI compound semiconductor crystals, its growth method, and semiconductor devices made of such crystals.

b) Description of the Rotated Art

[0003] Most of element semiconductors such as Si and Ge and group III-V compound semiconductors such as GaAs can be given n- or p-type conductivity by doping donor or acceptor impurities.

[0004] The nature capable of forming semiconductors of both n- and p-types is called bipolar. If group III-V compound semiconductor is used, p- and n-type semiconductors can be formed on the same substrate. By using group III-V compound semiconductor, semiconductor devices having a p-n junction such as light emitting diodes (LED) can be manufactured.

[0005] A forbidden bandwidth (bandgap: Eg) is a value specific to crystal.

[0006] A light emission wavelength λ is generally expressed by the following equation.

$$\lambda = 1240/Eg$$

where λ is a light emission wavelength (nm) and Eg (eV) is a forbidden bandwidth of semiconductor.

[0007] The value Eg determines the wavelength of inter-band emission light of crystal, i.e., an emission light color. Of group III-V compound semiconductor, GaAs having a relatively narrow Eg has a forbidden bandwidth Eg of 1.43 eV. The emission light wavelength of GaAs is 870 nm in the infrared range. Of group III-V compound semiconductor, AlP having a relatively broad Eg has a forbidden bandwidth Eg of 2.43 eV. The emission light wavelength of AlP is 510 nm which is green emission.

[0008] Most of group II-VI compound semiconductor have Eg larger than that of group III-V compound semiconductor. Therefore, light emission can be expected from blue to royal purple and to a ultraviolet range.

[0009] Generally, group II-VI compound semiconductor has high ionicity and is mono-polar. Namely, crystals of group II-VI compound semiconductor have generally only one of n- and p-type conductivities and crystals having both conductivities are rare.

[0010] Such mono-polar behavior can be explained by self-compensation.

[0011] For example, in group II-VI compound semiconductor crystals ZnS, a void of S negative ion having a smaller size has a smaller coupling energy than that of Zn positive ion having a larger size. The effect that Zn positive ion voids compensate p-type impurities is distinctive, and p-type ZnS is hard to be manufactured. Although the self-compensation effect changes with the type of group II-VI compound semiconductor, the phenomenon that p-type ZnO is hard to be manufactured can also be explained in the manner similar to ZnS. If p-type ZnO crystals can be obtained easily, various semiconductor devices using ZnO can be manufactured.

SUMMARY OF THE INVENTION

[0012] It is an object of the present invention to provide p-type group II-VI compound semiconductor crystals, more specifically a method of growing p-type ZnO crystals.

[0013] It is another object of the present invention to provide p-type group II-VI compound semiconductor crystals, more specifically p-type ZnO crystals and semiconductor devices using such crystals.

[0014] In this specification, material containing ZnO as its host element and ZnTe as its dopant or guest element is described simply as ZnO.

[0015] According to one aspect of the present invention, there is provided a method of growing p-type group II-VI compound semiconductor crystals, comprising a step of: forming ZnO layers and ZnTe layers alternately on a substrate, the ZnO layer being not doped with impurities and having a predetermined impurity concentration, and the ZnTe layer being doped with p-type impurities N to a predetermined impurity concentration or higher.

[0016] According to another aspect of the present invention, there is provided a p-type group II-VI compound semiconductor crystalline material, comprising: a lamination structure of ZnO layers and ZnTe layers alternately stacked on a substrate, wherein N is doped at least in the ZnTe layer.

[0017] According to another aspect of the present invention, there is provided a group II-VI compound semiconductor device comprising: a substrate; an n-type group II-VI compound semiconductor layer doped with group III elements and formed on the substrate; and a p-type group II-VI compound semiconductor layer formed on the substrate and having ZnO layers and ZnTe layers alternately laminated, N being doped at least in the ZnTe layer.

[0018] As above, p-type ZnO having good crystallinity and small electrical resistance can be grown.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

Fig. 1 is a schematic cross sectional view showing the outline of an MBE apparatus used with a crystal growth method according to a first embodiment of the invention.

Fig. 2 is a cross sectional view showing the superlattice structure of ZnO - N-doped ZnTe grown by the crystal growth method of the first embodiment of the invention.

Figs. 3A and 3B are timing charts showing the shutter control sequences of crystal growth methods of the first embodiment.

Fig. 4 is a cross sectional view showing the superlattice structure of ZnO - N-doped ZnTe grown by a crystal growth method according to a second embodiment.

Fig. 5 is a cross sectional view showing the structure of an LED device having a p-n junction diode using as p-type semiconductor a superlattice of ZnO - N-doped ZnTe grown by the crystal growth method of the second embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] Embodiments of the invention will be described with reference to the accompanying drawings.

[0021] With reference to Figs. 1 to Figs. 3A and 3B, a method of growing group II-VI compound semiconductor crystals according to the first embodiment of the invention will be described.

[0022] Fig. 1 shows a crystal growth apparatus using molecular beam epitaxy (MBE) (hereinafter called an "MBE apparatus"), as one example of apparatuses for growing group II-VI compound semiconductor crystals.

[0023] This MBE apparatus A has a chamber 1 in which crystals are grown and a vacuum pump 2 for maintaining the inside of the chamber 1 at a ultra high vacuum.

[0024] The chamber 1 has a Zn port 11 for evaporating Zn, a Te port 21 for evaporating Te, an O radical port 31 for irradiating O radical, and an N radical port 41 for irradiating N radical Te.

[0025] The Zn port 11 has a shutter S_1 and a Knudsen cell (hereinafter called a K cell) 17 for accommodating a Zn (purity 7N) source 15 and heating and evaporating Zn. The Te port 21 has a shutter S_2 and a K cell 27 for accommodating a Te (purity 6N) source 25 and heating and evaporating Te.

[0026] The O radical port 31 jets out O radical into the MBE chamber 1, the O radical being generated from oxygen gas introduced as source gas into an electrodeless discharge tube, by using a radio frequency (13.56 MHz). A shutter S_3 is provided for an O radical beam.

[0027] The N radical port 41 jets out N radical into the MBE chamber 1, the N radical being generated from nitrogen gas introduced as source gas into an electrodeless discharge tube, by using a radio frequency (13.56 MHz). A shutter S_4 is alto provided for an N radical beam.

[0028] In the chamber 1, a substrate holder 3 and a heater 3a are installed. The substrate holder 3 holds an underlie substrate S used for crystal growth, and the heater 3 heats the substrate holder 3. A temperature of the substrate S can be measured with a thermo couple 5. The position of the substrate holder 3 can be changed by a manipulator 7 using bellows.

[0029] The chamber 1 also has a reflective high energy electron diffraction (RHEED) gun 51 and an RHEED screen 55 provided for monitoring a grown crystal layer. By using the RHEED gun 51 and RHEED screen 55, crystals can be grown while the state (growth quantity and grown crystal layer quality) of crystal growth in the MBE apparatus A is monitored.

[0030] A controller C can properly control a crystal growth temperature, a grown crystal layer thickness, a vacuum degree in the chamber, and the like.

[0031] Processes of growing p-type ZnO on a ZnO substrate will be described in detail.

[0032] All crystal growth is executed by MBE.

[0033] A beam quantity of Zn is 1.5×10^{-7} Torr, and a Te beam quantity is 4.5×10^{-7} Torr.

[0034] As an oxygen beam source, an oxygen RF plasma source is used. O radical is generated from pure oxygen (purity 6N) introduced in to the O radical port 31, by using an RF oscillator.

[0035] As a nitrogen beam source, a nitrogen RF plasma source is used. N radical is generated from pure nitrogen (purity 6N) introduced in to the N radical port 41, by using an RF oscillator.

[0036] In the O radical port 31, the flow of oxygen gas is set to 2 ccm and the pressure thereof is set to 8×10^{-5} Torr. In the N radical port 41, the flow of nitrogen gas is set to 0.03 ccm and the pressure thereof is set to 2×10^{-6} Torr. The growth temperature is set to 600 °C.

[0037] These pressure values were measured with a nude ion gauge mounted at the substrate holder position (growth position).

[0038] The unit "ccm" used for the flow rate of gas source is a flow rate at 25 °C at one atmospheric pressure, as well known.

[0039] Fig. 2 is a cross sectional view of p-type ZnO crystal layers grown by the embodiment method. On a ZnO substrate 100, a superlattice layer 105 made of non-doped ZnO layers and N-doped ZnTe layers is grown. More specifically, the non-doped ZnO layer contains impurities smaller than a predetermined concentration, e.g., 1×10^{16} cm^{-3}, and the ZnTe layer contains impurities of a predetermined concentration, e.g., 1×10^{18} cm^{-3}.

[0040] The superlattice layer 105 is made of a lam-

ination of ZnO layers 101a, 101b,..., 101z and ZnTe layers 103a, 103b,..., 103z, alternately stacked. Each of the ZnO layers 101a, 101b,..., 101z has preferably a thickness of a two-molecule layer or thicker, e.g., a thickness of a ten-molecule layer. Each of the ZnTe layers 103a, 103b,..., 103z has a thickness of, e.g., a one-molecule layer, preferably a critical film thickness or thinner. On the ZnO substrate, a ZnO buffer layer may be formed on which the superlattice layer 105 is grown. The total thickness of the superlattice layer 105 is, for example, about 100 nm.

[0041] Figs. 3A and 3B illustrate two growth processes of growing ZnO crystal layers shown in Fig. 2, as open/close sequences of the shutters S_1 to S_4. Of the two growth processes, the growth process shown in Fig. 3A is called a first growth process, and the growth process shown in Fig. 3B is called a second growth process.

[0042] Referring to Fig. 3 showing the first growth process, the shutter S_1 for Zn and the shutter S_3 for O are opened at time t_1. Zn and O elements fly onto the surface of the substrate 100 and a ZnO crystal layer is grown. By controlling the growth parameters such as a Zn supply amount and an O supply amount, ZnO crystals are grown in the unit of a molecule layer.

[0043] In this specification, a one-molecule layer means a crystal unit constituted of a Zn one-atom layer and an O one-atom layer. Until a crystal layer having a thickness of a ten-molecule layer is grown, the shutters S_1 and S_3 are maintained open.

[0044] The shutter S_3 for O is closed at time t_2 to stop a supply of O_2 elements until time t_3 and supply only Zn elements. Since only Zn elements are supplied, the uppermost surface of the non-doped ZnO layer 101a is formed with a Zn-terminating surface. In order to remove excessive Zn elements, all the shutters are closed during a period from t_3 to t_4. At time t_4, the shutter S_2 for Te and the shutter T_4 for N are opened to supply Te and N elements to the Zn-terminating surface. Te and N elements are coupled with the Zn-terminating surface so that an N-doped ZnTe layer having a thickness of a one-molecule layer is grown.

[0045] The RHEED pattern of the ZnTe layer is (2x1) at time t_4 which shows a state of Te rich.

[0046] All the shutters are closed during a period from t_5 to t_6 to remove and degas surplus atoms. Thereafter, the shutter S_1 for Zn is opened again to adjust the terminating surface of ZnTe and change the surface of Te rich to a surface of Zn rich. The surface morphology and characteristics can therefore be improved.

[0047] Next, the shutter S_3 for O is opened at time t_7 to again grow ZnO. This state is same as the state at time t_1. The above processes are repeated 30 times.

[0048] With these processes, p-type ZnO crystals shown in Fig. 2 can be grown.

[0049] The outline of the second growth process shown in Fig. 3B will be described.

[0050] The shutter S_1 for Zn is opened to continuously supply Zn elements to the substrate. The shutter S_3 for O is opened at time t_1 to supply O elements and grow ZnO elements not doped with impurities to a desired concentration.

[0051] The shutter S_3 for O is closed at time t_2 to stop a supply of O elements. Thereafter, the shutter S_2 for Te and shutter S_4 for N are opened at time t_4 to supply Te and N elements and grow a ZnTe layer doped with N.

[0052] The shutters S_2, S_3 and S_4 are closed during a period from t_5 to t_6 to adjust the terminating surface of ZnTe.

[0053] Next, the shutter S_3 for O is opened at time t_7 to again grow ZnO. This state is same as that at time t_1. The above processes are repeated 30 times.

[0054] If the ZnO buffer layer 101 is formed as in the first growth process, Zn and O are supplied to the substrate 100 in advance to grow a ZnO layer having a desired thickness, and thereafter the above-described processes are performed.

[0055] The superlattice layer has a ratio of ZnO of a ten-molecule layer to ZnTe of a one-molecule layer, after the completion of each of the first and second growth processes. The bandgap of the laminated superlattice layer is approximately equal to that of ZnO.

[0056] ZnTe exhibits p-type conductivity as N impurities are doped. Impurity diffusion and hole motion from the N-doped ZnTe layer to the ZnO layer occur over the whole thickness of the ZnO ten-molecule layer.

[0057] The ZnO/ZnTe superlattice layer grown in the above manner exhibits p-type conductivity as a whole.

[0058] The thickness of ZnTe was set to a one-molecule layer. This thickness is a critical film thickness or thinner so that strain to be generated in the grown layer can be suppressed to a small amount. The surface morphology of the grown layer can be made good.

[0059] As a flow rate of N during growth of ZnTe is set to 0.05 ccm under the above-described conditions, the dope amount of N into ZnTe can be suppressed to 1 x 10^{20} cm^{-3}.

[0060] The concentration of impurities (N) entered in ZnO through diffusion or the like is preferably suppressed lower than the concentration of impurities (N) doped in ZnTe.

[0061] Fig. 4 is a cross sectional view showing the structure of p-type semiconductor using ZnO/ZnTe superlattice according to the second embodiment of the invention.

[0062] On a sapphire substrate 201, a ZnO layer 211 is grown to a thickness from 30 nm to 100 nm, e.g., 50 nm at a low temperature from 300 °C to 500 °C, e.g., 400 °C. The ZnO layer 211 grown at a low temperature has initially an amorphous state. The substrate is thereafter gradually heated. This heating progresses crystallization so that the ZnO layer grown at the low temperature changes to an epitaxial ZnO layer.

[0063] Next, a superlattice layer 225 of ZnO and N-doped ZnTe is grown to a total thickness of 100 nm by

the growth method similar to the growth method of the first embodiment.

[0064] In the crystalline structure shown in Fig. 4, the grown superlattice layer 225 has ZnO layers 201a, 201b,..., 201z and N-doped ZnTe layers 203a, 203b,..., 203y alternately laminated on the low temperature grown ZnO layer 211 formed on the sapphire substrate 201.

[0065] Since the low temperature grown ZnO layer 211 is intervened between the sapphire substrate 201 and superlattice layer 225, strain to be caused by a lattice coefficient difference between the sapphire substrate 201 and superlattice layer 225 can be relaxed. The surface morphology can be improved.

[0066] According to the above-described group II-VI compound semiconductor growth method, it is possible to grow p-type ZnO crystals having good crystallinity and low electrical resistance.

[0067] Fig. 5 is a cross sectional view showing the structure of an LED (Light Emitting Diode) having a p-n junction and formed by using n-type Ga-doped ZnO and by using superlattice made of ZnO - N-doped ZnTe as p-type semiconductor.

[0068] As shown in Fig. 5, LED has a sapphire substrate 301, a non-doped ZnO buffer layer 305 grown at a low temperature and having a thickness of 100 nm, an n-type (Ga doped: 1 x 10^{18} cm^{-3}) ZnO layer 311 formed on the layer 305 and having a thickness of 100 nm, and a superlattice layer 315 (total thickness of about 100 nm) formed on the layer 311 and made of 30 layers of ZnO and N-doped ZnTe alternately laminated.

[0069] The n-type ZnO layer 311 is made in contact with a first electrode 321.

[0070] The n-type ZnO layer may be formed by doping other group III elements such as Al instead of doping Ga.

[0071] The superlattice layer 315 is patterned to an island shape. The superlattice layer 315 patterned to the island shape has its outer peripheral area covered with an insulating film 318 made of, for example, SiN. An opening having a shape of, for example, an approximately circular shape, is formed through the insulating film 318 to expose the upper surface of the superlattice layer 315. The insulating film 318 covers and protects at least the side wall of the island-patterned superlattice layer 315.

[0072] A second electrode 325 having an opening, for example, a ring electrode, is formed on the upper circumferential area of the superlattice layer 315. The lower surface on the inner circumferential side of the ring-shaped second electrode 325 is in contact with the upper circumferential surface of the superlattice layer 315. The outer circumferential side of the second electrode rides on the insulating film 318.

[0073] With this structure, as a positive voltage is applied to the second electrode 325 relative to the first electrode 321, a forward current flows through the p-n junction. Minority carriers (electrons) injected into the p-type superlattice layer 315 and majority carriers (holes) in the p-type super lattice layer 315 are recombined radiatively. When electrons and holes recombine, light having an energy approximately equal to an energy gap of the forbidden band is radiated from the above-described opening. Namely, electric energy is converted into optical energy.

[0074] With the above-described operation, light having a wavelength of about 370 nm is emitted from the opening of LED. Although this LED has the p-type superlattice layer as the optical surface (light emission surface), it is obvious that it may have an n-type superlattice layer as the optical surface (light emission surface).

[0075] In this embodiment, LED is used as an example of a semiconductor device using a p-n junction between the p-type superlattice layer 315 (ZnO and N-doped ZnTe) and the n-type ZnO. Obviously, a laser device by using a combination of the p-type superlattice layer 315 and n-type ZnO may be formed. It is also obvious that a combination with the p-type superlattice layer 315 can manufacture electronic devices such as FETs and bipolar transistors, other optical devices, and semiconductor devices made of a combination of these devices.

[0076] The present invention has been described in connection with the preferred embodiments. The invention is not limited only to the above embodiments. For example, the thickness of each thin film constituting the superlattice layer may be changed as desired so long as desired characteristics can be satisfied. The gas supply sequences are not limited to those described above. The growth conditions and other process parameters can be selected in various ways. It is apparent that various modifications, improvements, combinations, and the like can be made by those skilled in the art.

Claims

1. A method of growing p-type group II-VI compound semiconductor crystals, comprising a step of:

   forming ZnO layers and ZnTe layers alternately on a substrate, the ZnO layer being not doped with impurities and having a predetermined impurity concentration, and the ZnTe layer being doped with p-type impurities N to a predetermined impurity concentration or higher.

2. A method of growing p-type group II-VI compound semiconductor crystals according to claim 1, wherein each ZnTe layer is grown to a thickness of a critical film thickness or thinner.

3. A method of growing p-type group II-VI compound semiconductor crystals according to claim 1, wherein each ZnO layer is grown to a thickness of a two-molecule layer or ticker.

4. A method of growing p-type group II-VI compound semiconductor crystals according to claim 1, wherein:

a process of forming the ZnO layer comprises the steps of:

(a) supplying Zn and O elements to the substrate;
(b) after said step (a), stopping a supply of O elements; and
(c) after said step (b), stopping a supply of Zn elements to remove excessive Zn elements above the substrate; and

a process of forming the ZnTe layer comprises the steps of:

(d) after said step (c), supplying Te and N elements; and
(e) after said step (d), stopping a supply of Te and N elements to the substrate to intercept crystal growth on the substrate.

5. A method of growing p-type group II-VI compound semiconductor crystals according to claim 4, further comprising the steps of:

(f) after said step (e), supplying Zn elements to the substrate; and

(g) after said step (f), supplying O elements to the substrate.

6. A method of growing p-type group II-VI compound semiconductor crystals according to claim 1, wherein:

a process of forming the ZnO layer comprises, in a state that Zn elements are supplied to the substrate, the steps of:

(a) supplying O elements to grow the ZnO layer not doped with impurities and having the predetermined impurity concentration; and
(b) after said step (a), stopping a supply of O elements; and

a process of forming the ZnTe layer comprises the steps of:

(c) after said step (b), supplying Te and N elements to grown the ZnTe layer doped with N.

7. A p-type group II-VI compound semiconductor crystalline material, comprising:

a lamination structure of ZnO layers and ZnTe layers alternately stacked on a substrate, wherein N is doped at least in the ZnTe layer.

8. A p-type group II-VI compound semiconductor crystalline material according to claim 7, wherein the ZnO layer is doped with N at a lower concentration than an N concentration doped in the ZnTe layer.

9. A p-type group II-VI compound semiconductor crystalline material according to claim 7, further comprising a ZnO layer grown at a low temperature formed between the lamination structure and the substrate.

10. A group II-VI compound semiconductor device comprising:

a substrate;
an n-type group II-VI compound semiconductor layer doped with group III elements and formed on the substrate; and
a p-type group II-VI compound semiconductor layer formed on the substrate and having ZnO layers and ZnTe layers alternately laminated, N being doped at least in the ZnTe layer.

11. A group II-VI compound semiconductor device according to claim 10, further comprising:

a first electrode electrically connected to said n-type group II-VI compound semiconductor layer; and
a second electrode electrically connected to said p-type group II-VI compound semiconductor layer.

12. A group II-VI compound semiconductor device according to claim 11, wherein an opening is formed through one of said first and second electrodes to expose a surface of said n-type or p-type group II-VI compound semiconductor layers.

13. A group II-VI compound semiconductor device according to claim 10, further comprising a ZnO layer grown at a low temperature in contact with the substrate.

14. A group II-VI compound semiconductor device according to claim 11, further comprising a ZnO layer grown at a low temperature in contact with the substrate.

FIG.1

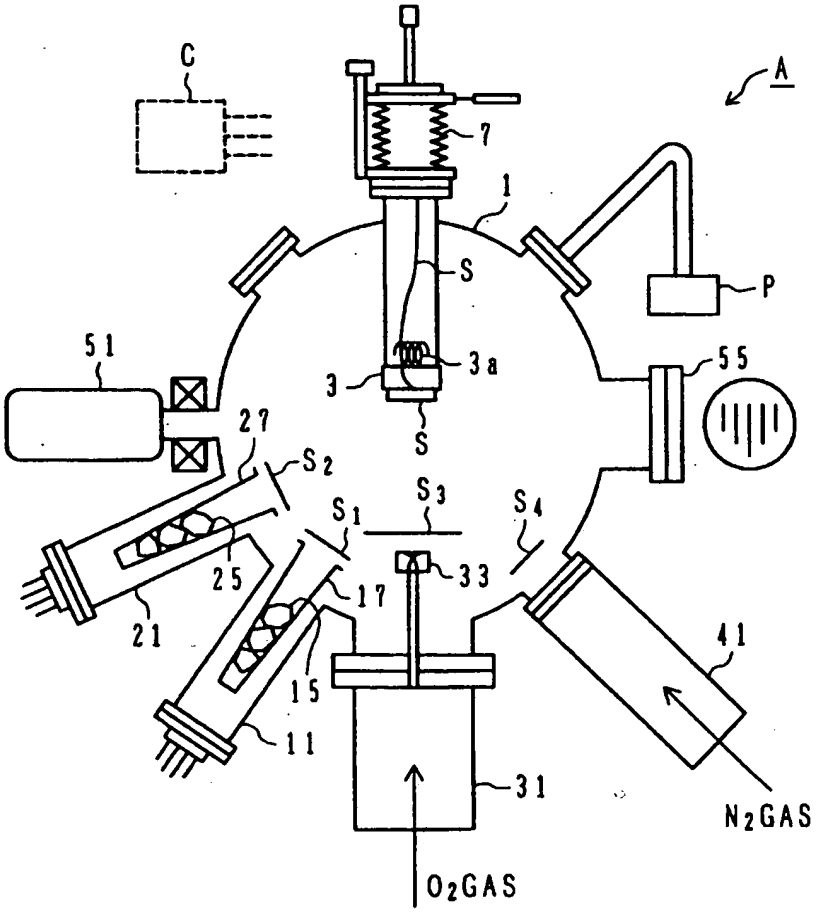


FIG.2

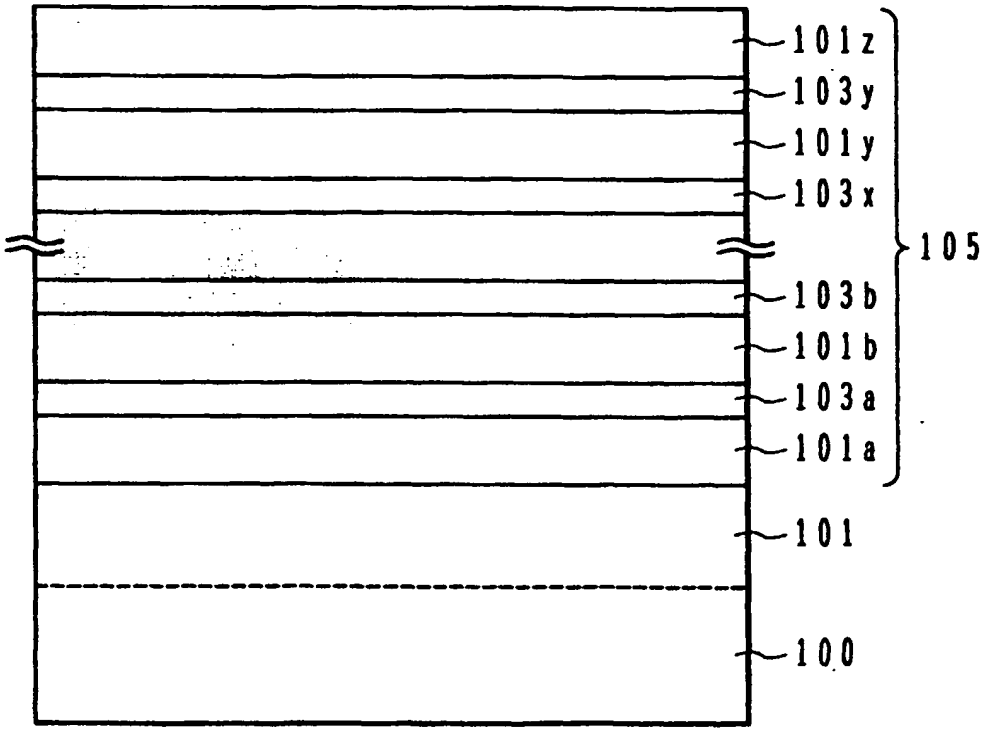


FIG.3A

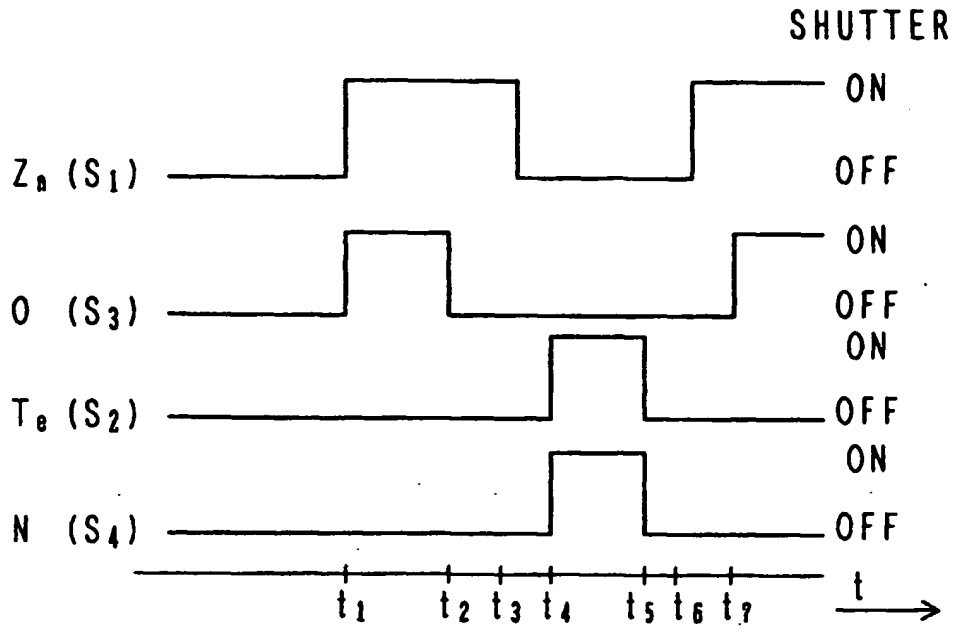


FIG.3B

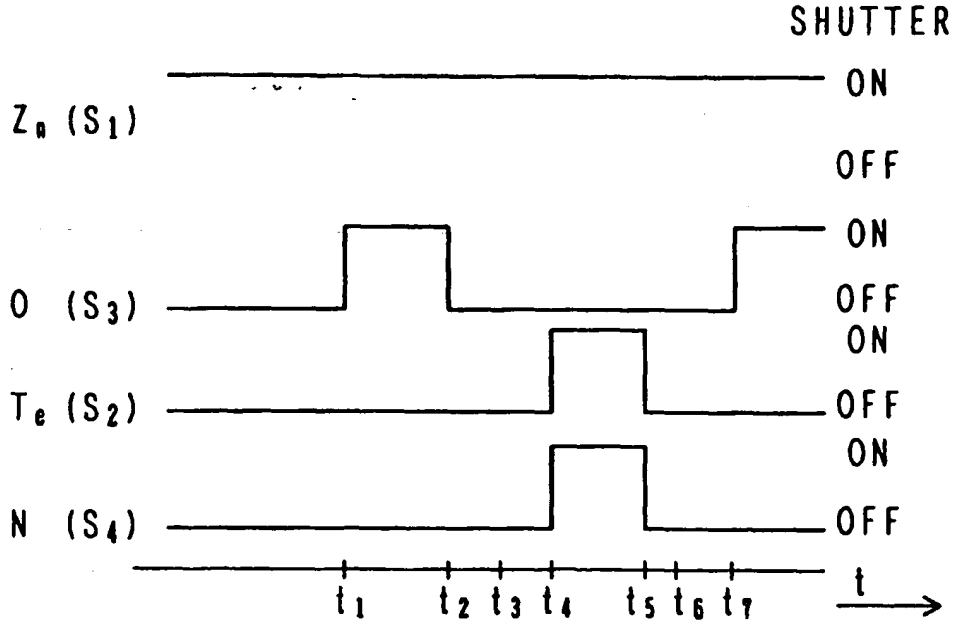


FIG.4

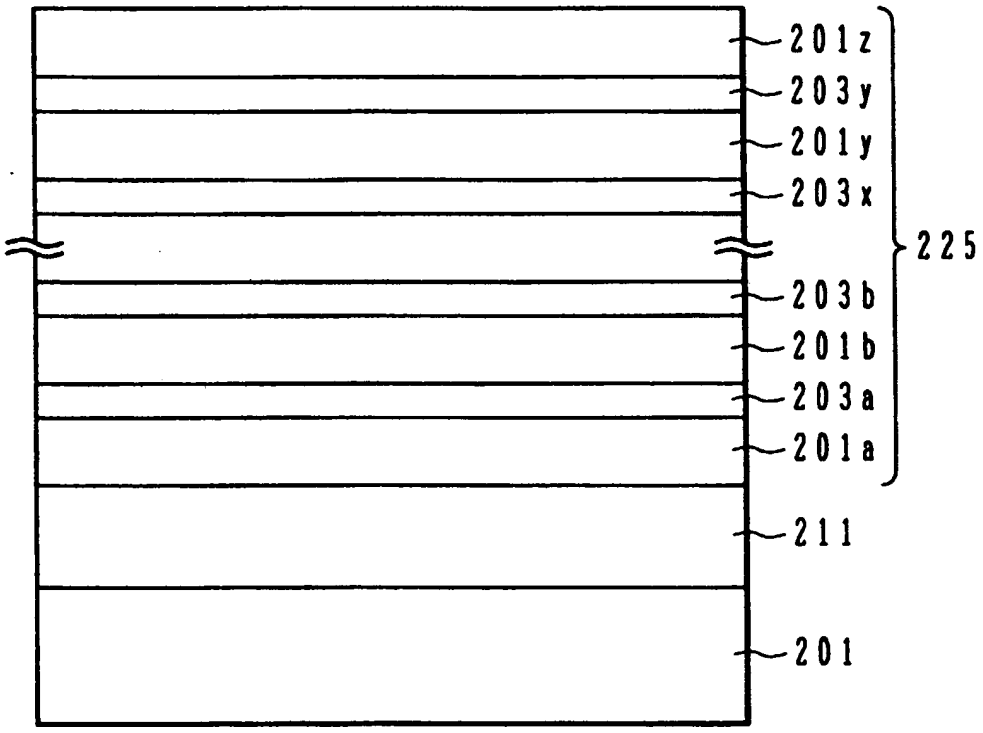
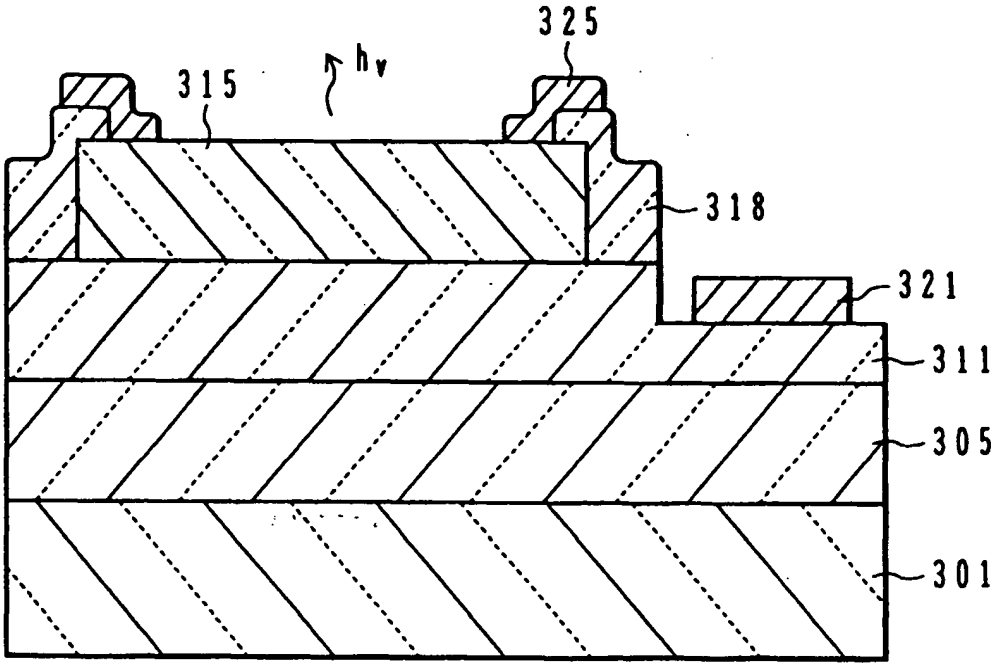


FIG.5



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 11 0829

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 August 2000	Cook, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 11 0829

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